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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/037,485	12/19/2001	Ubaldo Mastromatteo	854063.665	5220

500 7590 12/04/2002

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EXAMINER
VU, HUNG K

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 12/04/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/037,485	Applicant(s) MASTROMATTEO, UBALDO
	Examiner Hung K. Vu	Art Unit 2811

-- Th MAILING DATE of this communication app ars on the cov r sheet with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 October 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12 and 30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-9 and 30* is/are rejected.

7)☒ Claim(s) *4 and 10-12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election of Invention of Group II, Claims 1-12 and 30, in Paper No. 7 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Applicant's election without traverse of Invention of Group II, Claims 1-12 and 30, in Paper No. 7 is acknowledged.

Claim Objections

2. Claims 4 and 5 are objected to because of the following informalities:

In claim 4, line 5, delete " (2)" for clarity.

In claim 5, line 3, "(of" should be changed to "of" for clarity.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 5 and 8 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the

invention. The independent claim 1 recites the limitations of Figures 1-7, and dependent claims 5 and 8 recited the limitations of Figures 10-12. The inventor is not allowed to claim the combination of two different figures into a single group of claims.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 30 is rejected under 35 U.S.C. 102(b) as being anticipated by Temple et al. (PN 5,654,226).

Temple et al. discloses, as shown in Figure1, 2D, 2E and 3-4, a process for manufacturing an integrated device comprising,

forming integrated structures (emitters 16 which are part of the bipolar transistors) in a first wafer (10) of semiconductor material (silicon), the first wafer including an exposed semiconductor region (16);

forming a bonding layer (18,32) of a metal material on a second wafer (12) of semiconductor material (silicon);

bonding the first and second wafers together by causing the bonding to react with the semiconductor region. Note Col. 3, lines 45-50, Temple et al. teaches that metal puts on the surface of the wafer and anneals to form the silicide. Therefore, it is inherent that the bonding layer (metal) will react the semiconductor region (16) to form the silicide.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 6-7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Temple (PN 5,654,226) in view of Yu et al. (PN 5,801,083).

Temple discloses, as shown in Figure1, 2D, 2E and 3-4, a process for manufacturing an integrated device comprising,

forming integrated structures (emitters 16 which are part of the bipolar transistors) including semiconductor regions in a first wafer (10) of semiconductor material (silicon);

forming interconnection structures (18,32) of conductor material on a second wafer (12) of semiconductor material (silicon), including forming plug elements (18) each having a bonding region of a metal material capable of reacting with the semiconductor regions of the first wafer;

bonding the first wafer and the second wafer together, including causing the bonding regions to react with the semiconductor regions. . Note Col. 3, lines 45-50, Temple et al. teaches that metal puts on the surface of the wafer and anneals to form the silicide. Therefore, it is inherent that the bonding layer (metal) will react the semiconductor region (16) to form the silicide.

Temple et al. does not disclose isolation regions form in the first wafer. However, Yu et al. discloses a plurality of isolation regions (9,10) form in a wafer (1). Note Figure 8 of Yu et al..

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the device of Temple et al. having a plurality of isolation regions form in the first wafer, such as taught by Yu et al. in order to isolate integrated structures from each others to prevent the short circuit between integrated circuits.

With regard to claim 2, Temple et al. and Yu et al. disclose the semiconductor material is silicon, and the step of causing the bonding region to react comprises forming a metal silicide. Note Col. 3, line 31-50 of Temple et al..

With regard to claim 3, Temple et al. and Yu et al. disclose the metal material is chosen from among titanium, tungsten and platinum. Note Col. 3, line 45-50 of Temple et al..

With regard to claim 6, Temple et al. and Yu et al. disclose the step of forming interconnection structures comprises forming electrical connection regions of conductive material (16), and the step of forming plug elements comprises forming base regions (lower portion of 18,32) of conductive material on top of and in direct electrical contact with the electrical connections regions, and forming the bonding regions (upper portion of 18,32) on top of the base regions.

With regard to claim 7, Temple et al. and Yu et al. disclose the step of forming integrated structures comprises forming integrated electronic components (emitters 16 which are part of the bipolar transistors).

With regard to claim 9, Temple et al. and Yu et al. does not disclose before the step of bonding the first and second wafers comprising the step of forming self-alignment structures on the first and second wafers, and aligning the first and second wafers, using the self-alignment structures. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the device of Temple et al. and Yu et al. further comprising a step of forming self-alignment structures on the first and second wafers, and aligning the first and second wafers, using the self-alignment structures because this step is a conventional step to use for alignment two wafers before bonding to prevent misalignment between the bonding regions and the semiconductor regions.

Allowable Subject Matter

6. Claims 4 and 10-12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is an examiner's statement of reasons for allowance:

Applicant's claims 4 and 10-12 are allowable over the references of record because none of these references disclose or can be combined to yield the claimed invention such as the plug elements have a height, and the step of forming integrated structures comprises forming an insulating material layer on top of a substrate of semiconductor material, the insulating material layer having a thickness smaller than the height of the plug elements, and forming openings in the insulating material to uncover selective portions of the substrate, and wherein the step of

bonding the first and second wafers comprises causing the bonding region to react with at least the selective portions of the substrate, as recited in claim 4, and the step of forming self-alignment structures comprises forming at least one engagement seat in one of the firs and second wafers, and forming at least one engagement element on another of the first and second wafers in a position facing the engagement seat, as recited in claim 10.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hung K. Vu whose telephone number is (703) 308-4079. The examiner can normally be reached on Mon-Thurs 7:00-4:30 and every other Friday 7:00-3:30, Eastern Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Vu

November 29, 2002

Hung Vu